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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/192,651	11/16/98	FUEHRER	T 2-9-24-11

EXAMINER	
SINGH, R	
ART UNIT	**PAPER NUMBER**
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DATE MAILED: 03/14/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/192,651	FUEHRER ET AL.	
	Examiner	Art Unit	
	Dr. Ramnandan Singh	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 1998* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 1998* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings filed on 16 November 1998 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required.

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hein et al [US 6,198,816 B1] in view of Hershbarger et al [US 5,654,984] , and further in view of Kan et al [US 6,020,773].

The central piece of the instant invention is to utilize clock signals to charge capacitors used for high voltage digital isolation in a telephone interface circuit. In this process, large capacitors are used to form a charge pump to generate power to interface circuits. Based the same principle, Hein et al teaches generating power for phone interface circuits having capacitor-coupled isolation barriers [fig. 2 (element 220)].

Regarding claim 1 , Hein et al teaches an interface circuit comprising a data access arrangement (DAA) (Fig. 2) and a charge pump (Figs. 5 (element 532)) providing operating power to the DAA [Figs. 1-15; col. 1, lines 28-67; col. 2, lines 1-67; col. 3, lines 1-67; col. 4, lines 1-67; col. 6, lines 1-45; col. 8, lines 1-67; col. 9 to col. 18; col. 24, lines 49-67; col. 25 to col. 29]. Further, different types of digital signal processor (DSP) are commercially available from either Motorola or Texas Instruments, Inc. and are utilized to integrate subsystems into a system in the art.

Regarding claim 2, Hein et al teaches the interface circuit wherein the charge pump comprises a first capacitive element (Fig. 2 (element 209))and an a second capacitive element(fig. 2(element210)) having an input and an output each connected

to the DAA; and a rectifying element (Fig. 2 (element 640)) coupled between the output side of the first capacitive element and the second capacitive element .

Regarding claim 3, Hein et al teaches the interface circuit wherein a clock recovery for generating a two-phase non-overlapping clock signal (Fig. 2 (element 216) ; Fig. 7. (element 707)); and the first capacitive element comprises: a first capacitor coupled to receive the first clock pulse; a second capacitor Coupled to receive the second clock pulse, wherein the first capacitive element continuously outputs a positive output voltage to the rectifying element [Figs.2, 3A, 3B, 4A, 4B, 5, 6A, 6B, 8-14].

Regarding claim 4, Hein et al teaches the interface circuit wherein the rectifying element comprises a diode rectifier [Fig. 2 (element 640)].

Regarding claim 5, Hein et al teaches the interface circuit wherein the DAA includes a clock regeneration element connected in parallel with the rectifying circuit to remove DC level shift and regenerate a clock pulse for use by the DAA which is essentially identical to the clock pulse output by the clock generator.[Fig. 2; (element 216;) Fig. 7. (element 707)].

Regarding claim 6, Hein et al teaches the interface circuit wherein the second capacitive element comprises a storage capacitor which stores the charge transferred by the first and the second capacitors. [Fig. 5 (element 534)].

Hein et al does not teach expressly a digital signal processor (DSP) incorporating controlling and processing of all subsystems., and a clock generator generating first and second clock pulses out of phase with each other by 180 degrees.

Hershbarger et al teaches a DSP for use with a charge pump for high voltage isolation for a DAA system [Figs. 2, 7(elements 704 and 705), 9, 10; col. 2, lines 59-67; col. 3, lines 1-29; col. 6, lines 7-13; col. 14, lines 45-67; col. 15, lines 1-67; col. 16, lines1-28].

Kan et al discloses a clock signal generator for generating a plurality of clock signals with different phases and clock phase controller using the same [Figs. 1-14; col. 3, lines 29-67; col.4, lines 1-47].

Hein et al , Hein et al and Hershbarger et al are analogous art because they are from a similar problem solving area, viz., using clock signals with capacitors .

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the DSP implementation of Hershbarger et al and the clock pulse generation and control of Kan et al with the Hein et al system.

The suggestion/motivation for doing so would have been to enhance power generation of the charge pump of Hein et al by integrating various subsystems of Hein et al using a DSP, and the clock generator and controller of Kan to ensure sufficient power for high speed modems with computers in the user premises meeting the FCC regulation requirements for a telephone interface in the U.S.

Therefore, it would have been obvious to combine Hershbarger et al and Kan et al with Hein et al to obtain the invention as specified in claims 1-6.

5.. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hein et al , Hershbarger et al, and Kan et al as applied to claims 1-6 in paragraph 4 supra.

Regarding claim 7, Hein et al teaches a method of providing power to a data access arrangement (DAA) in an interface circuit of a telecommunication network when a telephone line connected to the interface circuit is in the on-hook state, the interface circuit including a digital signal processor (DSP) having a clock generator, the method comprising the steps of: inserting a charge pump between the DSP and the DAA; generating a power signal across the charge pump by inputting the output of the clock

generator to the charge pump; and storing the generated power signal for use by the interface [Figs. 1-21; col. 24, lines 51-57; col. 25-36].

All the limitations of this claim has already been demonstrated in para 4 above.

6. Claims 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hein et al [US 6,198,816 B1] in view of Hershbarger et al [US 5,654,984] , and further in view of Kan et al [US 6,020,773].

Regarding claim 8 , Hein et al teaches an interface circuit comprising a driver circuit for developing a charge across capacitive elements of the interface circuit; a data access arrangement (DAA) (Fig. 2) and a charge pump (Figs. 5 (element 532)) providing operating power to the DAA [Figs. 1-21; col. 1, lines 28-67; col. 2, lines 1-67; col. 3, lines 1-67; col. 4, lines 1-67; col. 6, lines 1-45; col. 8, lines 1-67; col. 9 to col. 18; col. 24, lines 49-67; col. 25 to col. 29]. Further, a digital signal processor (DSP) is commercially available in the market and is used to integrate subsystems into a system.

Regarding claim 9, Hein et al teaches the interface circuit wherein the charge pump comprises a first capacitive element (Fig. 2 (element 209))and an a second capacitive element(fig. 2(element 210)) having an input and an output each connected to the DAA; and a rectifying element (Fig. 2 (element 640)) coupled between the output side of the first capacitive element and the second capacitive element .

Regarding claim 10, Hein et al teaches the interface circuit wherein a clock recovery for generating a two-phase non-overlapping clock signal (Fig. 2; element 216; Fig. 7. (element 707)); and the first capacitive element comprises: a first capacitor coupled to receive the first clock pulse; a second capacitor Coupled to receive the second clock pulse, wherein the first capacitive element continuously outputs a positive output voltage to the rectifying element [Figs.2, 3A, 3B, 4A, 4B, 5, 6A, 6B, 8-14].

Regarding claim 11, Hein et al teaches the interface circuit wherein the rectifying element comprises a diode rectifier [Fig. 2 (element 640)].

Regarding claim 12, Hein et al teaches the interface circuit wherein the DAA includes a clock regeneration element connected in parallel with the rectifying circuit to remove DC level shift,and regenerate a clock pulse for use by the DAA which is essentially identical to the clock pulse output by the clock generator.[Fig. 2; (element 216;) Fig. 7. (element 707)].

Regarding claim 13, Hein et al teaches the interface circuit wherein the second capacitive element comprises a storage capacitor which stores the charge transferred by the first and the second capacitors. [Fig. 5 (element 534)].

Hein et al does not teach expressly a digital signal processor (DSP) incorporating controlling and processing of all subsystems., and a clock generator generating first and second clock pulses with each other by 180 degrees.

Hershbarger et al teaches a DSP for use with the charge pump for high voltage isolation for a DAA system [Figs. 2, 7(elements 704 and 705), 9, 10; col. 2, lines 59-67; col. 3, lines 1-29; col. 6, lines 7-13; col. 14, lines 45-67; col. 15, lines 1-67; col. 16, lines1-28].

Kan et al discloses a clock signal generator for generating a plurality of clock signals with different phases and clock phase controller using the same [Figs. 1-14; col. 3, lines 29-67; col.4, lines 1-47].

Hein et al , Hein et al and Hershbarger et al are analogous art because they are from a similar problem solving area, viz., using clock signals with capacitors .

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the DSP implementation of Hershbarger et al and the clock pulse generation and control of Kan et al with the Hein et al system.

The suggestion/motivation for doing so would have been to enhance power generation of the charge pump of Hein et al by integrating various subsystems of Hein

et al using a DSP, and the clock generator and controller of Kan to ensure sufficient power for high speed modems meeting the FCC regulation requirements for a telephone interface in the U.S.

Therefore, it would have been obvious to combine Hershbarger et al and Kan et al with Hein et al to obtain the invention as specified in claims 8-13.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Alternatively, (i) Rahamimi et al [US 6,081,586] for a DAA; (ii) Shimizu et al [US 6,049,238] for clock generation and control.; and (iii) Yurgelites [US 5,500,895] for capacitive isolation for a DAA.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Ramnandan Singh whose telephone number is (703)308-6270. The examiner can normally be reached on M-F(8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester Isen can be reached on (703)-305-4386. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-5403 for regular communications and (703)306-5631 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

Dr. Ramanandan Singh

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March 9, 2001

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